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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,249	11/25/2003	Kenichi Osada	H-1123	4095

7590 03/09/2006
MATTINGLY, STANGER & MALUR, P.C.
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ALEXANDRIA, VA 22314

EXAMINER

WEISS, HOWARD

ART UNIT PAPER NUMBER

2814

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/720,249

Applicant(s)

OSADA ET AL.

Examiner

Howard Weiss

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30-December-2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 9-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1103</u> . | 6) <input type="checkbox"/> Other: _____ |

Attorney's Docket Number: H-1123

Filing Date: 11/25/03

Continuing Data: none

Claimed Foreign Priority Date: 12/9/02, 11/11/03 (JPX)

Applicant(s): Osada et al. (Kawahara, Yamaoka)

Examiner: Howard Weiss

Election/Restrictions

1. Applicant's election of Specie I, Claims 1 to 8, in the reply filed on 12/30/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 9 to 21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected specie, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/30/05. Applicant is requested to cancel the non-elected claims as part of a complete response to this office action. Cancellation of the non-elected claims would not preclude the later filing of a divisional application on the non-elected invention (please see 35 USC 120 and 121).
3. Applicant's assertion that Claim 1 is generic is not found to be persuasive. In general, a generic claim should require no material element additional to those required by the species claims, and each of the species claims must require all the limitations of the generic claim. In this case, Claim 1 requires the channels of the first to fourth MISFETs be floating and the channels of the fifth and sixth MISFETs be coupled to the first wiring line. Neither Claims 9 nor 15 require these limitations. Additionally, Claim 1 does not require any of the elements in Claims 9 and 15. See MPEP § 806.04(d).

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 and 6 to 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katz (U.S. Patent No. 3,521,242) and Yamada (U.S. Patent No. 5,986,924).

Katz shows most aspects of the instant invention (e.g. Figure 8) including:

- a plurality of word **36** and bit **30a,b** lines
- a plurality of memory cells (see Figure 9)
- each cell consisting of (1,2) p-channel load transistors **14,22**, (3,4) n-channel driver transistors **12,20** and (5,6) n-channel transfer transistors **92,32**
- where the gate and channel regions of transistors (1-4) are not coupled together and the channel regions are floating
- drains of (1,3) are connected to the gates of (2,4) and drains of (2,4) are connected the gates of (1,3) and the source/drain path of (5,6) are connected to respective bit lines

Katz does not show the channels of (5,6) coupled to their respective gates and to a first wiring line. Yamada teaches (e.g. Figure 1) to couple the channels of transfer transistors **21,22** to a first wiring line **WLO** and the respective gates to improve the read/write speed of the memory cell. It would have been obvious to a person of ordinary skill in the art at the time of invention to couple the channels of transfer transistors to a first wiring line and the respective gates as taught by Yamada in the device of Katz to improve the read/write speed of the memory cell.

In reference to the claim language referring to the supplied voltages and potentials to word and bit lines and other features of the memory cell, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

6. Claims 2 to 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katz and Yamada, as applied to Claim 1 above, and further in view of Kotani (U.S. Patent No. 6,638,799).

Katz and Yamada show most aspects of the instant invention (Paragraph 5) except the memory device being on a chip with a first and second semiconductor layers are separated by an insulating layer and (1-6) transistors' diffusing layers are formed in said first semiconductor layer with the channel regions separated by an insulating layer. Kotani teach (e.g. Figure 1) to form n- and p-channel transistors **Rnt,Rpt** on a chip with a first **5** and second **3** semiconductor layers are separated by an insulating layer **4** and the transistors' diffusing layers **19** are formed in said first semiconductor layer with the channel regions **14,22** separated by an insulating layer **6** to fix a body electrical potential (Column 5 Lines 18 to 26). It would have been obvious to a person of ordinary skill in the art at the time of invention to form n- and

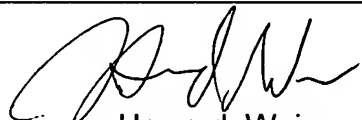
p-channel transistors on a chip with a first and second semiconductors layers are separated by an insulating layer and the transistors' diffusing layers are formed in said first semiconductor layer with the channel regions separated by an insulating layer as taught by Kotani in the device of Katz and Yamada to fix a body electrical potential. Additionally, it is obvious to use vertical transistors since they are common in SRAM devices.

Conclusion

8. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 7:00 AM to 3:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on **(571) 272-1705**.
10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **(866) 217-9197** (toll-free).

10. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/ 369; 365/156	2/28/06
Other Documentation: PLUS Analysis Report	8/26/05
Electronic Database(s): EAST, IEL	2/28/06



Howard Weiss
Primary Examiner
Art Unit 2814

31 August 2005